USN | | | | | | | | | | |

10EC/TE71

Seventh Semester B.E. Degree Examination, June/July 2017

Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the ISO-OSI reference model with a neat diagram. Discuss the function of each layer. **(10 Marks)**

b. Explain the signaling system seven (SS7) protocol with a neat diagram. **(05 Marks)**

c. Match the following functions to the appropriate layers in the OSI model:
i) Interface to the transmission media.
ii) Dividing the transmitted bit stream into frames
iii) Route determination
iv) Reliable process to process message delivery
v) Format and code conversion services **(05 Marks)**

2 a. Explain the bit stuffing and unstuffing by taking a suitable example. **(05 Marks)**

b. Explain the configuration modes of HDLC protocol with neat diagrams. **(05 Marks)**

c. Explain the stop and wait protocol with neat diagram. **(10 Marks)**

3 a. Explain the procedure for pure aloha protocol with a neat diagram. **(06 Marks)**

b. A slotted aloha network transmits 200 bit frames using a shared channel of 200 kbps bandwidth. Find the throughput, if the system produces,
i) 1000 frames per second
ii) 500 frames per second
iii) 250 frames per second **(06 Marks)**

c. Explain the working of CSMA/CD with a neat diagram. **(08 Marks)**

4 a. Compare the data rates for standard Ethernet, fast Ethernet, gigabit Ethernet and ten gigabit Ethernet. **(04 Marks)**

b. Identify whether the following Mac addresses are unicast, multicast or broad cast.
i) 4A : 30 : 10 : 21 : 10 : 1A
ii) 47 : 20 : 1B : 2E : 08 : EE
iii) FF : FF : FF : FF : FF : FF **(06 Marks)**

c. What are the common standard Ethernet implementation? Explain with neat diagrams. **(10 Marks)**

PART – B

5 a. Explain each of the following in brief:
i) Passive hub
ii) Repeater
iii) Bridge
iv) Router
v) Gateway **(10 Marks)**

b. Explain each of the following in brief :
i) Bus backbone networks
ii) Star backbone networks **(06 Marks)**

c. What is vlan? Explain. **(04 Marks)**

6 a. Explain the IPV4 datagram format with a neat diagram. **(10 Marks)**
b. Explain the classful addressing schemes. **(06 Marks)**
c. A block of addresses is granted to an organization. If the IP address of one of the host is 205.16.37.39/28, find the first address and last address in the block. **(04 Marks)**

7 a. What is the difference between a direct delivery and indirect delivery? **(04 Marks)**
b. What is multicasting? Explain with a neat diagram and mention the applications of multicasting. **(08 Marks)**
c. Classify the four types of links defined by OSPF and explain. **(08 Marks)**

8 a. Explain the TCP segment format with a neat diagram. **(10 Marks)**
b. What are the three domains of the domain name space? Explain. **(06 Marks)**
c. How does recursive resolution differ from the iterative resolution? **(04 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC/TE72

Seventh Semester B.E. Degree Examination, June/July 2019

Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What are the advantages of optical fiber communication? **(04 Marks)**

b. What is Numerical Aperture? Derive an expression for Numerical Aperture and Maximum acceptance angle in the case of step index optical fiber in terms of refractive indices of core and cladding material. **(10 Marks)**

c. Compare step index fiber with Graded index fiber. **(06 Marks)**

2 a. Explain different types of attenuation in optical fiber. **(08 Marks)**

b. Derive an expression for the pulse spread due to material dispersion using group delay concept. **(06 Marks)**

c. A step index multimode fiber with a Numerical aperture of a 0.20 supports approximately 1000 modes at an 850 nm wavelength.

i) What is the diameter of its core?

ii) How many does the fiber support at 1320 nm and 1550 nm?

iii) What percent of the optical power flows in the cladding in each case? **(06 Marks)**

3 a. Give comparison between LASER and LED. **(06 Marks)**

b. i) With the diagram, describe the operation of surface emitting LED.

ii) Explain the working of PIN photo detector with diagrams. **(10 Marks)**

c. A given Silicon Avalanche photo diode has a quantum efficiency of 65% at a wavelength of 900 nm. Suppose 0.5 μ Watt of optical power produces a multiplied photocurrent of 10 μA. Find the primary photocurrent and multiplication factor. **(04 Marks)**

4 a. Show that the optical power coupled into a step index fiber from an LED with Lambartian distribution is $P = P_S(NA)^2$ for $r_s \leq a$ with usual notations. **(07 Marks)**

b. What are the principal requirements of good connectors? Explain the different types of connectors. **(09 Marks)**

c. A GaAs optical source with a refractive index of 3.6 is coupled to a silica fiber that has a refractive index of 1.48. Calculate the optical power loss in dB at the joints when the fiber end and the source are in close physical contact. **(04 Marks)**

PART – B

5 a. Draw a signal path through a digital link with relevant components and electrical waveforms at every stage. **(06 Marks)**

b. Draw and explain the two types of front end amplifiers in optical fiber communication. **(06 Marks)**

c. Draw and explain eye pattern and mark the fundamental measurement parameter. **(08 Marks)**

6 a. What is link power budget? Explain the link power budget with a relevant diagram. **(06 Marks)**

b. Explain subcarrier multiplexing, with neat block diagram. **(06 Marks)**

c. What is rise time budget? Explain its significance. Derive an expression for the system rise time budget in terms of transmitter, fiber and receiver rise time. **(08 Marks)**

7 a. Explain the Wavelength Division Multiplexing (WDM) network containing various types of optical amplifiers. **(08 Marks)**

b. Explain the optical isolator with a design and operation of a polarization independent isolator mode of three miniature optical components. **(06 Marks)**

c. Explain the operation of optical Add/Drop multiplexer, with a relevant diagram. **(06 Marks)**

8 Write short notes on:

a. EDFA amplifier **(07 Marks)**

b. SONET/SDH **(07 Marks)**

c. Optical amplifier **(06 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC73

Seventh Semester B.E. Degree Examination, June/July 2019

Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

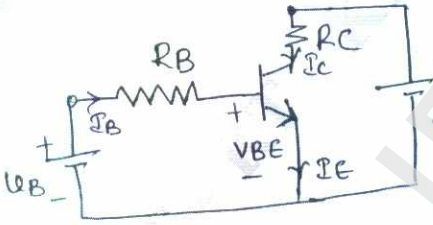
1 a. Explain five types of power electronic converter circuits briefly. Also indicate two applications of each type. **(10 Marks)**

b. Give symbol, and characteristic features of the following devices:
i) RCT ii) GTO iii) Triac iv) SCR v) IGBT **(10 Marks)**

2 a. Give the comparison between BJT, MOSFET and IGBT. **(06 Marks)**

b. What is the necessity of base drive control in a power transistor? Explain antisaturation control. **(08 Marks)**

c. For a transistor switch shown in Fig.Q2(c):
i) Calculate the forced beta, β_f of transistor.
ii) If the manufacturers specified β is in the range of 8 to 40, calculate the minimum overdrive factor (ODF)
iii) Obtain power loss P_T in the transistor.



$V_B = 10V$, $R_B = 0.75\Omega$
$V_{BE(sat)} = 1.5V$
$R_C = 11\Omega$, $V_{CC} = 200$ V
$V_{CE(sat)} = 1V$

Fig.Q2(c) **(06 Marks)**

3 a. Draw the two transistor model of a thyristor and derive an expression for the anode current in terms of the common base current gain α_1 and α_2 of the transistors. **(09 Marks)**

b. What is the need for protection of thyristor? Explain how thyristors are protected against high $\frac{di}{dt}$. **(06 Marks)**

c. Explain different methods to turn on a thyristor. **(05 Marks)**

4 a. What will be the average power in the load for the circuit shown in Fig.Q4(a), when $\alpha = \frac{\pi}{4}$. Assume SCR to be ideal. Supply voltage is 330 sin 314t. Also calculate the RMS power and the rectification efficient.

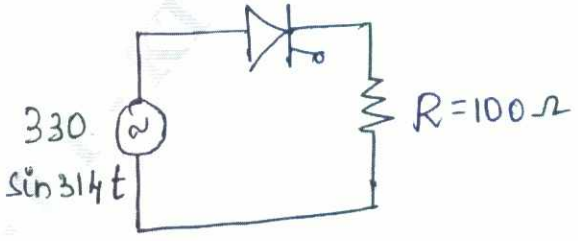


Fig.Q4(a) **(06 Marks)**

b. With a neat circuit diagram and waveforms, explain the working of a single phase full controlled bridge converter feeding highly inductive load. Derive the expression for the average output voltage and rms output voltage. **(10 Marks)**

c. Compare full controlled and semi-controlled rectifiers. **(04 Marks)**

PART – B

5 a. With a neat circuit diagram and waveforms, explain complementary commutation. **(10 Marks)**

b. In the resonant pulse commutation circuit, the supply voltage is is $V_S = 200$ V, load current $I_o = 150$ A, the commutation inductance $L = 4\mu H$ and commutation capacitance $C = 20\ \mu F$. Determine the peak resonant reversing current of thyristor T_3 and turn OFF time t_{OFF} for T_1. Assume $V_O = V_S$. **(10 Marks)**

6 a. With relevant circuit and waveform, explain the principle of single phase fullwave AC voltage controller with resistive load. Derive expression for RMS output voltage. **(10 Marks)**

b. A single phase FW ac voltage controller working on ON-OFF control has supply voltage of 230 V RMS, 50 Hz and load is 50 Ω. The controller is ON for 30 cycles and OFF for 40 cycles. Calculate:
   i) ON or OFF time interval
   ii) RMS output voltage
   iii) Input power factor
   iv) Average and RMS thyristor current **(06 Marks)**

c. Compare ON-OFF controller and phase controller. **(04 Marks)**

7 a. Give the classification of choppers. Explain briefly each one of them. **(10 Marks)**

b. Explain the working of boost regulator with waveforms. **(06 Marks)**

c. Explain the principle of operation of step up chopper. **(04 Marks)**

8 a. Explain the performance parameters of inverters. **(06 Marks)**

b. Explain the operations of single phase half bridge inverter. **(08 Marks)**

c. Explain the working of variable DC link inverter. **(06 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC74

Seventh Semester B.E. Degree Examination, June/July 2019

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is an embedded system? Explain with an example in detail. **(05 Marks)**

b. With a block diagram explain the various components in a microprocessor based embedded system. **(07 Marks)**

c. Briefly describe the major elements of the embedded system development life cycle with a flow chart. **(08 Marks)**

2 a. Explain with block diagram four major blocks of an embedded Hardware core and typical bus structure comprising Address, Data and Control Signals. **(05 Marks)**

b. Explain following addressing modes with an example for each:
i) Immediate mode
ii) Direct and indirect modes
iii) Indexed mode
iv) Program counter relative mode **(08 Marks)**

c. Write the block diagram of RTN model for a microprocessor data path and memory interface. Also explain fetch, execute and next control operations with RTL instructions. **(07 Marks)**

3 a. Explain the internal diagram of SRAM and write the timing diagram for read operation. **(07 Marks)**

b. Explain associative mapping cache implementation. **(06 Marks)**

c. With respect to dynamic memory allocation, explain :
i) Swapping
ii) Overlays
iii) Multiprogramming. **(07 Marks)**

4 a. With a flow diagram briefly explain the V cycle model and the spiral life cycle model. **(06 Marks)**

b. Write hardware architecture and data and counter flow diagram of a counter system and briefly explain flow diagram. **(08 Marks)**

c. Explain the characterizing and identifying the requirements of a system with respect to a digital counter. **(06 Marks)**

PART – B

5 a. Explain the following:
i) The CPU is a resource
ii) Lightweight and heavy weight threads
iii) A Single thread
iv) Multiple threads **(08 Marks)**

b. Describe virtual machine model and high level model for OS architecture. **(06 Marks)**

c. Discuss task control block. Mention some of the major components of task control also write C declarations for task control block. **(06 Marks)**

6 a. Explain the following:
   i) Basic diagram of possible task states
   ii) Reentrant code
   iii) Foreground/Background systems **(06 Marks)**

   b. Write the algorithm for a simple OS Kernel using C language notation for 3 asynchronous tasks sharing a common data buffer. **(08 Marks)**

   c. Explain the following:
   i) Duplicate hardware context
   ii) Runtime stack
   iii) Application stack **(06 Marks)**

7 a. Write the Amdahl's law for performance improvement/optimization. Consider a system with the following characteristics. The task to be analyzed and improved currently executes in 100 time units and the goal is to reduce execution time to 80 time units. The algorithm under consideration in the task uses 40 time units. Determine unknown parameter value in the equation and write the inference. **(07 Marks)**

   b. Write a 'c' function to determine sum of elements in an array and analyze it line by line for its time proximity. **(07 Marks)**

   c. Analyze the following:
   i) For loops
   ii) While loops
   iii) Conditional statements **(06 Marks)**

8 a. Write and analyze linear search algorithm for its time complexity. **(07 Marks)**

   b. Write and analyze selection sort algorithm for its time complexity. **(07 Marks)**

   c. Describe memory loading with equation, figure and an example. **(06 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC751

Seventh Semester B.E. Degree Examination, June/July 2019
DSP Algorithm and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List and explain the commonly found unique architectural features implemental in programmable DSP devices. **(04 Marks)**

b. A simple FIR filter where output is the average of the current input x[n] and the past input x[n – 1] and given by ;
$y[n] = 0.5\, x[n] + 0.5\, x[n-1]$
Draw the block diagram for the above equation. Find unit impulse, frequency response, magnitude response, and phase response of this filter. Also find the group delay and sketch magnitude and phase response curves. **(10 Marks)**

c. Explain with block diagram and equation the DSP operations ;
i) Decimation ii) Interpolation. **(06 Marks)**

2 a. Investigate the basic features that should be provided in the DSP architecture to be used implement the following N^{th} order FIR filter :

$$y[n] = \sum_{i=0}^{N-1} h[i]x[n-i] \quad n = 0, 1, 2, \ldots\ldots$$

Where x[n] denotes the input sample ; y[n] the output sample ; and h[i]the i^{th} filter coefficient x[n – i] is the input sample i samples earlier than x[n]. **(08 Marks)**

b. Explain circular addressing mode used in DSP device with algorithm and an example. **(08 Marks)**

c. It is required to find the sum of 64 numbers each represented by 16-bits. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error? If accumulator is only of 16-bits, how many bits should each number be shifted before the addition to prevent overflow? What is the actual sum of number, if all numbers are fixed-point integers? What is the error in the computation of sum? **(04 Marks)**

3 a. Explain with example, the following addressing modes of TMS320C54XX processors :
i) Immediate addressing ii) Absolute addressing
iii) Accumulator addressing iv) Memory – mapped register addressing. **(08 Marks)**

b. If the contents of AR3, BK and ARO are 1040h, 45h and 0050h respectively, then find starting and ending address for the buffer when AR3 is selected as the pointer for the circular buffer. Also find the content of register AR3 after the execution of the following instructions :
i) *AR3 + 0 ii) * + AR3(– 40h) iii) *AR3 + 0B iv) LD*AR3 + 0%, A. **(06 Marks)**

c. Explain program control unit of TMS320C54XX processors. **(06 Marks)**

4 a. Explain the following instructions of TMS320C54XX processor with examples :
i) MPY ii) MAC iii) MAS iv) RPT. **(08 Marks)**

b. Write a program using TMS320C54XX processors instruction set to compute the sum of three product terms given by the equation.
$y[n] = h_0\, x[n] + h_1\, x[n-1] + h_2\, x\,[n-2]$
where x[n], x[n – 1] and x[n – 2] are data samples stored at three successive date memory locations and h_0, h_1 and h_2 are constants stored at three other successive locations in the data memory. The result y[n] is to be stored in the data memory. Use direct addressing made to access the data memory. **(06 Marks)**

c. With a neat diagram explain hardware timer circuit of TMS320C54XX processors. **(06 Marks)**

PART – B

5 a. Explain Q-notations technique used in DSP algorithm implementation. **(04 Marks)**

b. What values are represented by the 16-bit fixed point number N = 3333h in the Q_{15}, Q_8, Q_5, and Q_1 notations. **(04 Marks)**

c. With the help of block diagram, explain the implementation of an IIR filter in TMS320C54XX processors. **(06 Marks)**

d. Write a set of instructions to implement FIR filter in TMS320C54XX processors. **(06 Marks)**

6 a. Explain, how scaling present overflow conditions in the butterfly computation. **(06 Marks)**

b. Determine the following for a 128 point FFT computation :
i) Number of stages
ii) Number of butterflies in each stage
iii) Number of butterflies needed for the entire computation
iv) Number of butterflies that need no twiddle factors
v) Number of butterflies that require real twiddle factors
vi) Number of butterflies that require real complex twiddle factors. **(06 Marks)**

c. With an 8-point FFT implement structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processor using ¼ as a scaling factor for all butterflies. **(08 Marks)**

7 a. With timing diagram, explain read – write operation of memory interface signals. **(06 Marks)**

b. Design a data memory system with address range 000800h-000FFFh for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

c. Classify the interrupts and explain the interrupt handling sequence by the C54XX processors with a flow chart. **(08 Marks)**

8 a. Explain in detail with timing diagrams the synchronous serial interface of C54XX DSP. **(10 Marks)**

b. Explain DSP – based bio-telemetry receiver system with block diagram. Also explain the PPM (Pulse Position Modulation) encoding and decoding scheme used in biotelemetry receiver system. **(10 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC/TE762

Seventh Semester B.E. Degree Examination, June/July 2019
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What is real time? Explain how real time system are divided with respect to time constraints with examples. **(08 Marks)**

b. Explain : i) clock based tasks ii) Event based tasks **(06 Marks)**

c. Explain : i) sequential programming ii) multitask programming iii) real time programming. **(06 Marks)**

2 a. Explain DDC with a neat figure and list the advantages of DDC over analog control. **(08 Marks)**

b. Explain sequence control and illustrate the same with a simple chemical reactor vessel. **(06 Marks)**

c. List out the responsibilities of a control engineer in designing the suitable computer system. **(06 Marks)**

3 a. Explain with a neat diagram analog output interface. **(05 Marks)**

b. With a diagram, explain digital input interface. **(06 Marks)**

c. Explain communications and the ways of characterizing serial. **(06 Marks)**

Draw a single chip computer and explain. **(03 Marks)**

4 a. Explain the following : i) Security ii) Readability iii) Portability. **(09 Marks)**

b. Explain exception handling. **(06 Marks)**

c. Explain co-routines. **(05 Marks)**

PART – B

5 a. Explain scheduling strategies. **(05 Marks)**

b. List the functions of task management, explain task states with a task state diagram. **(08 Marks)**

c. Explain :
i) Task chaining and swapping
ii) Task overlaying. **(07 Marks)**

6 a. Explain mutual exclusion using binary semaphore. **(07 Marks)**

b. Explain semaphore. **(05 Marks)**

c. What is Liveness? Explain. **(08 Marks)**

7 a. Explain software design in case of preliminary design of RTSS with diagram. **(08 Marks)**

b. Explain multitasking approach. **(04 Marks)**

c. With flow chart explain foreground/background approach. **(08 Marks)**

8 a. Explain Yourdon methodology. **(05 Marks)**

b. Show the outline of abstract modeling approach of ward and Mellor and explain. **(08 Marks)**

c. Explain the CFDO drying oven controller using Hately and Pirbhai notation. **(07 Marks)**

* * * * *